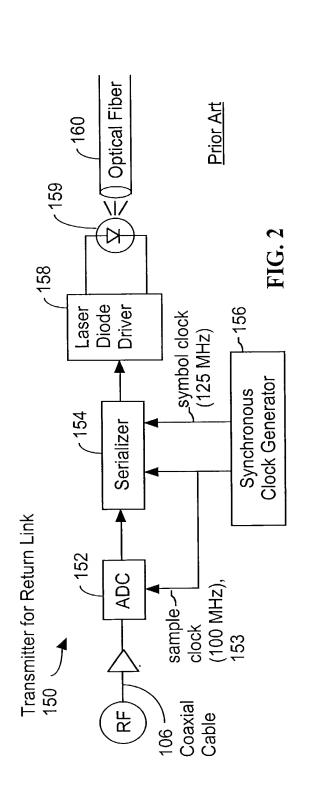
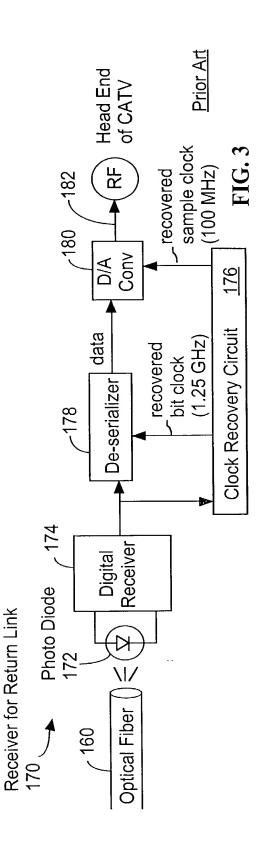
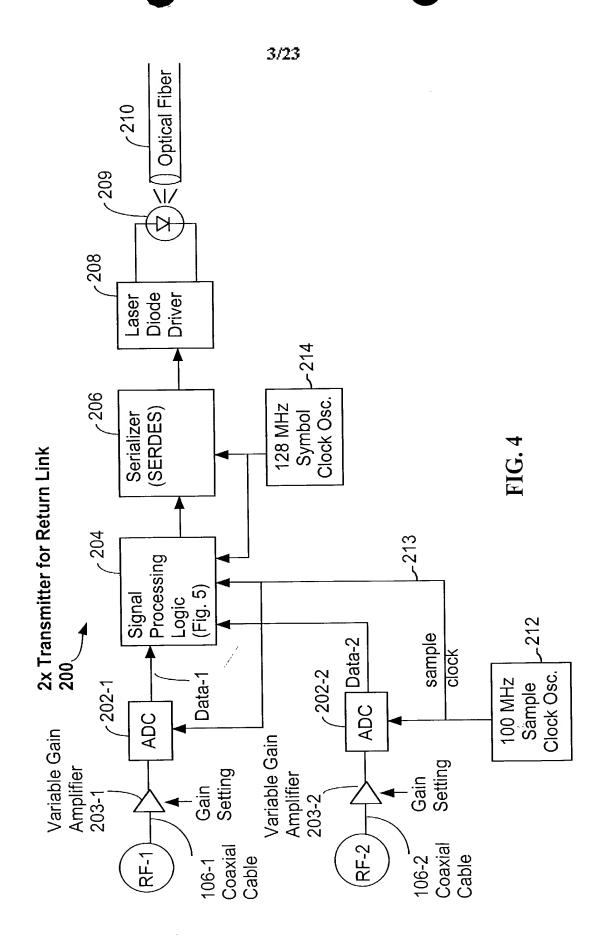
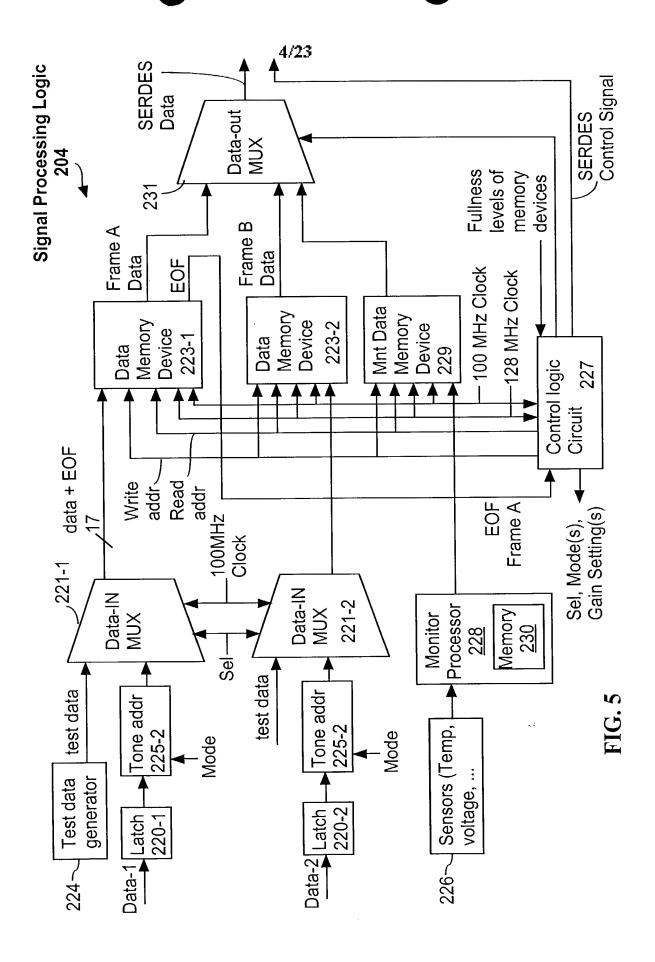
FIG. 1









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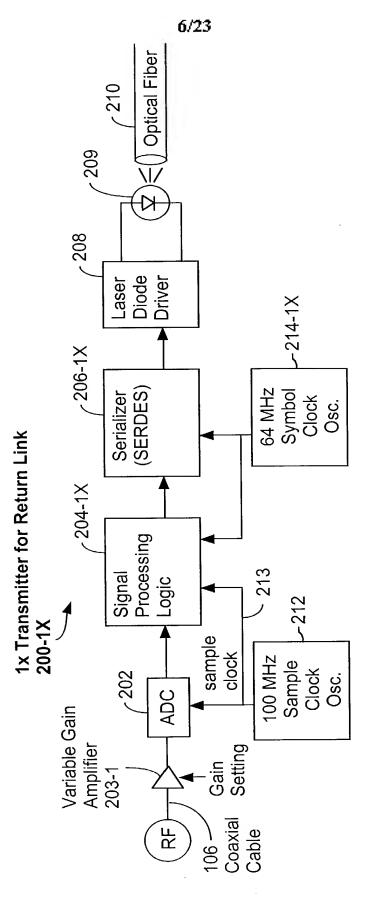
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FIG. 6A

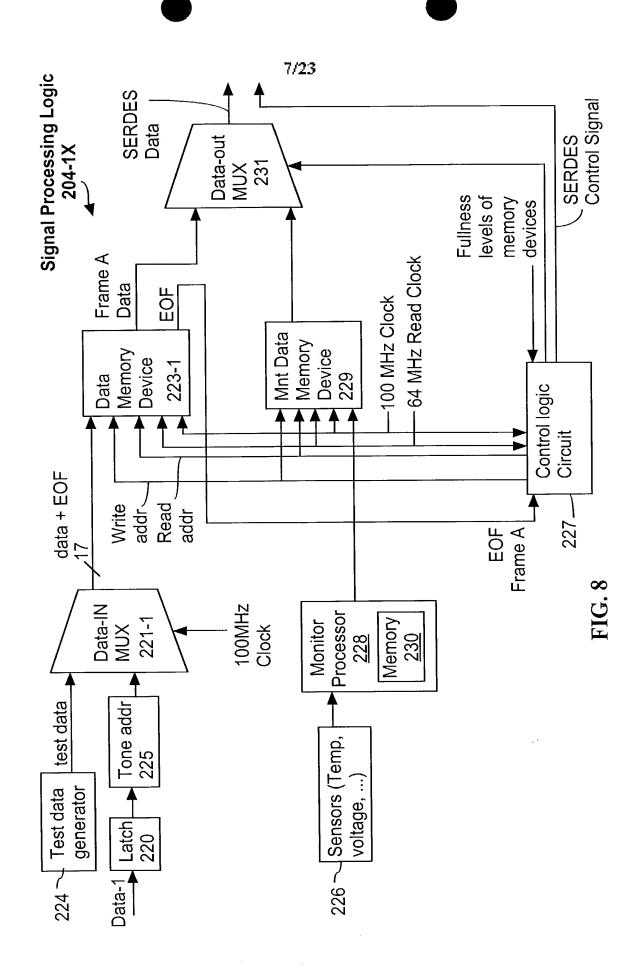
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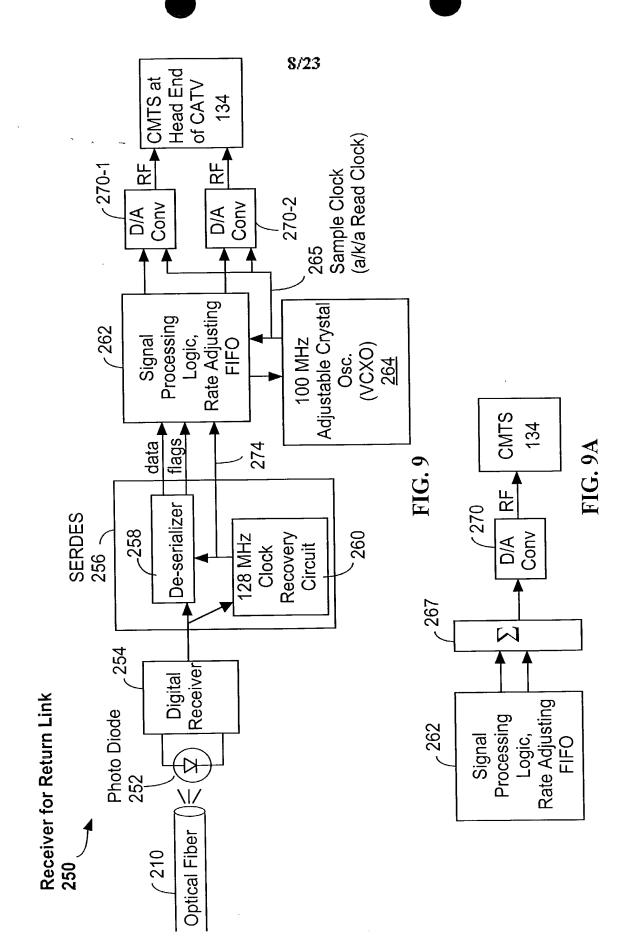
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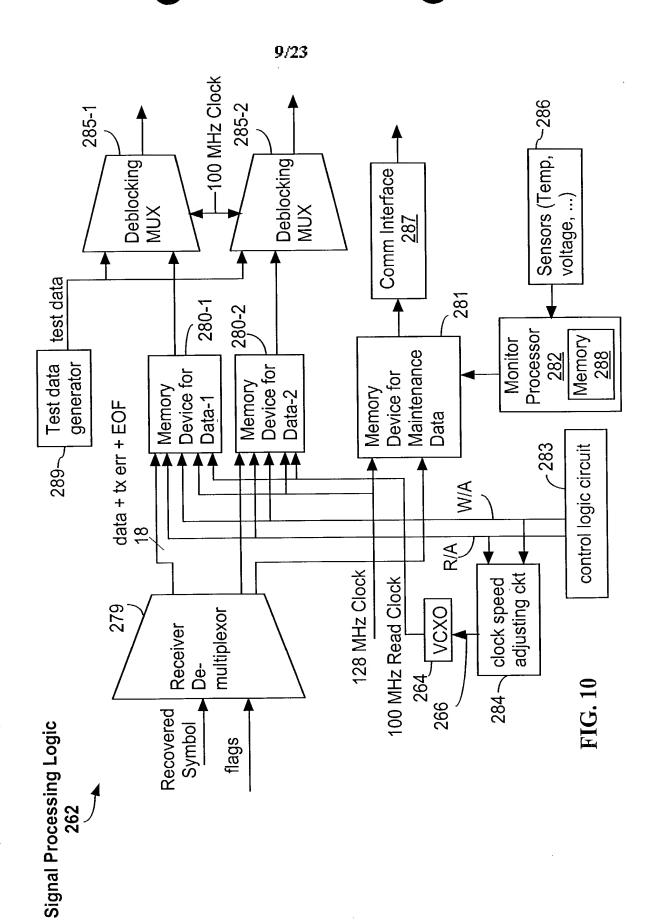
Ç

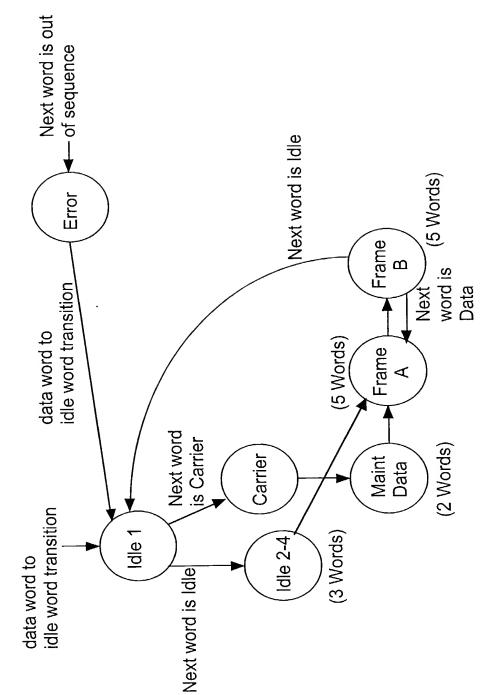


**FIG. 7** 



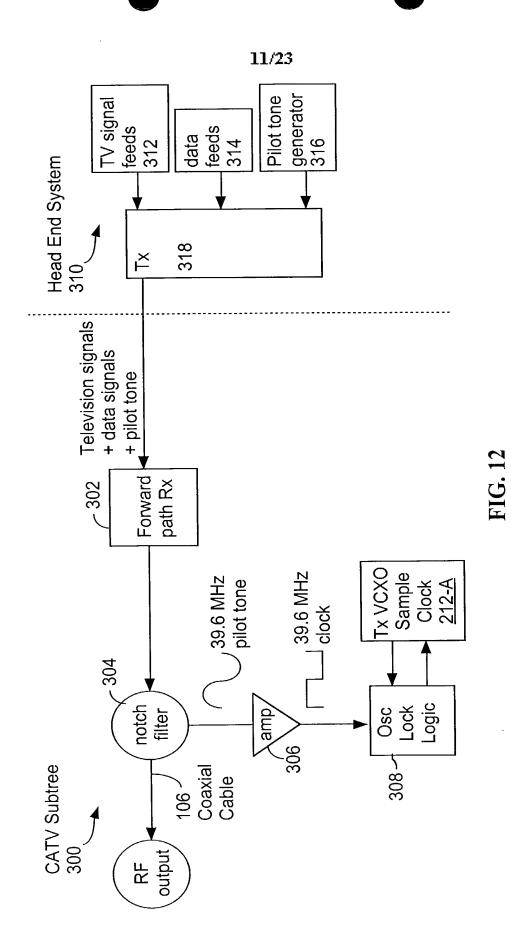






State Diagram for Dual Channel Receiver Demultiplexor

FIG. 11



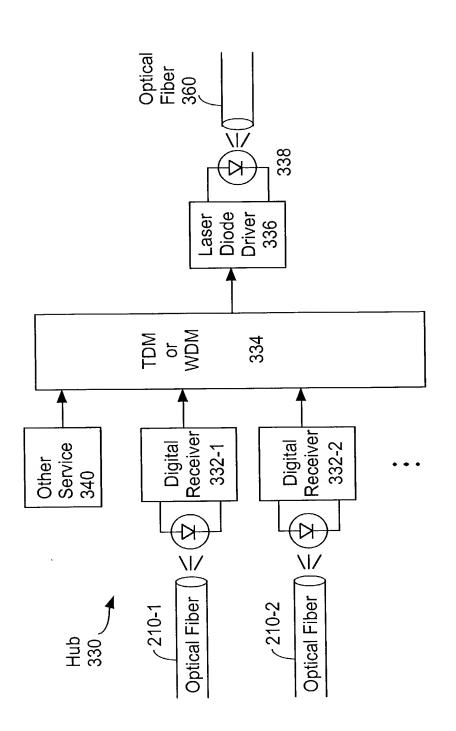


FIG. 13

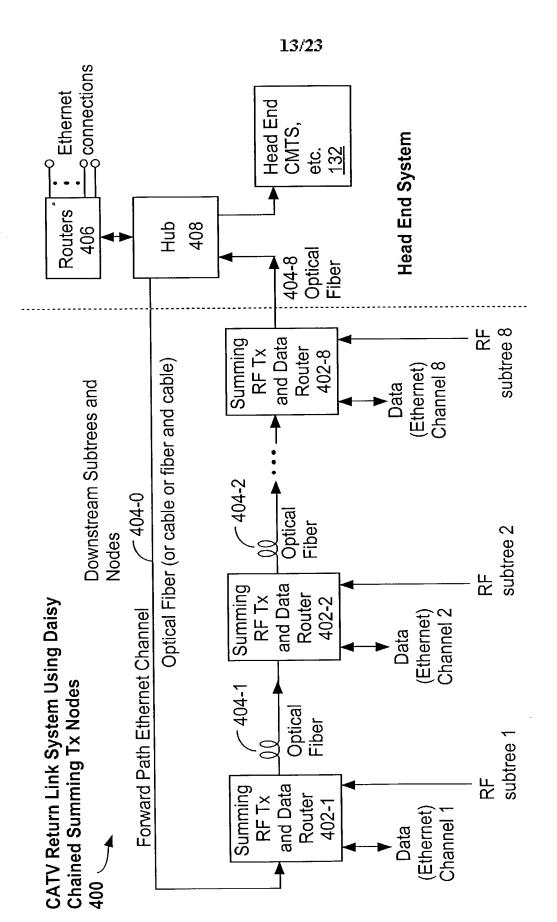


FIG. 14

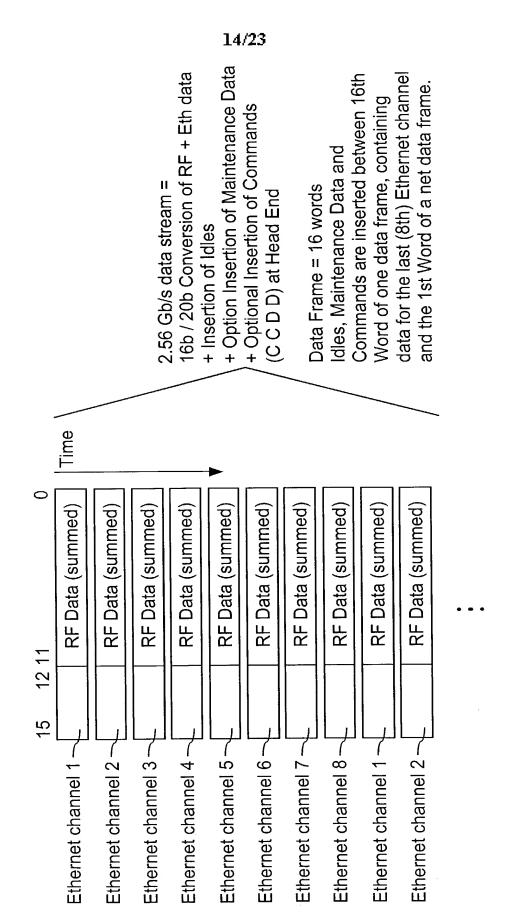
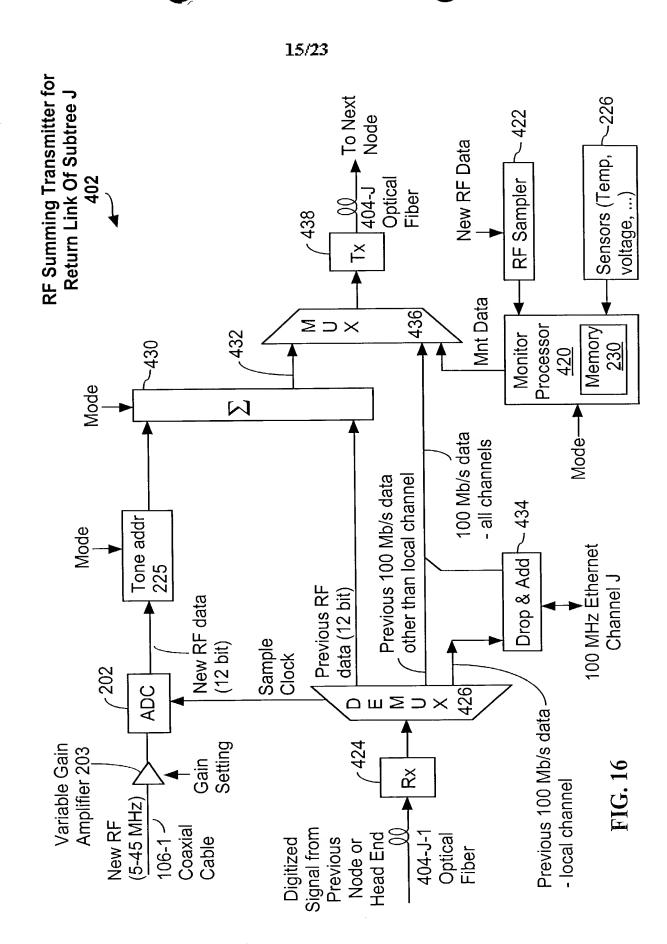


FIG. 1



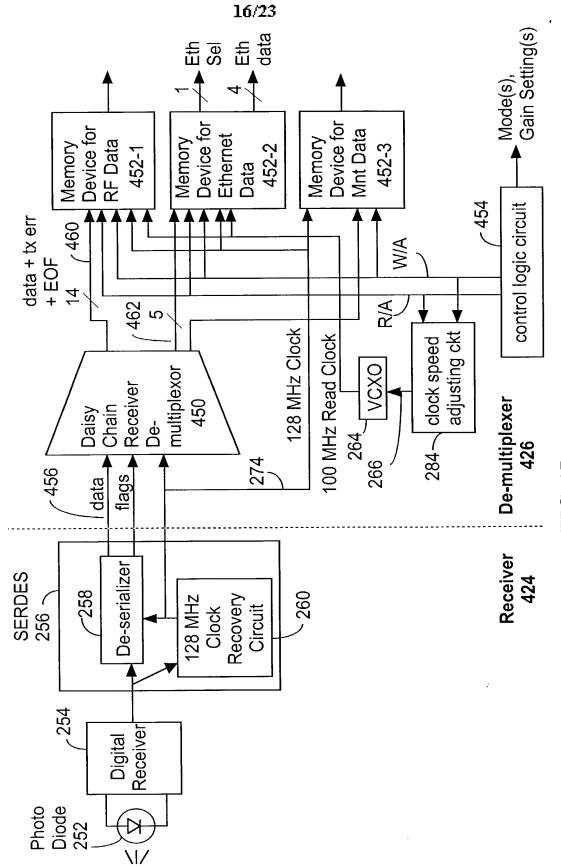


FIG. 17

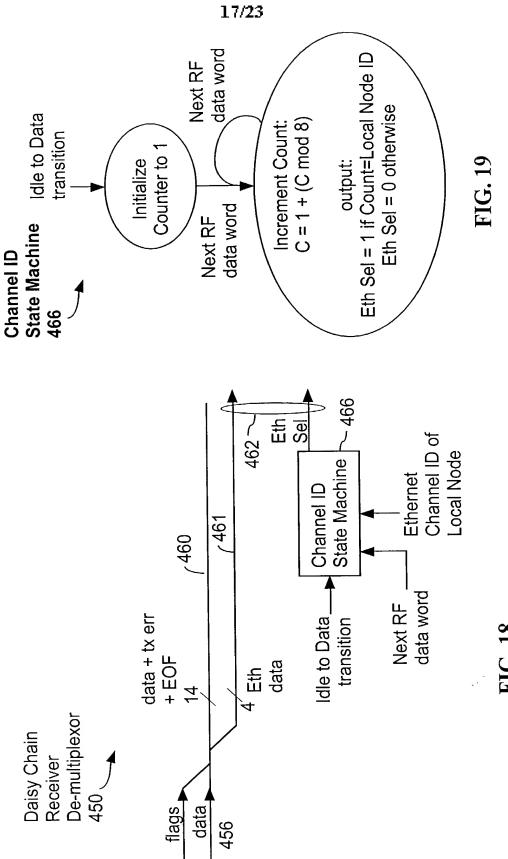
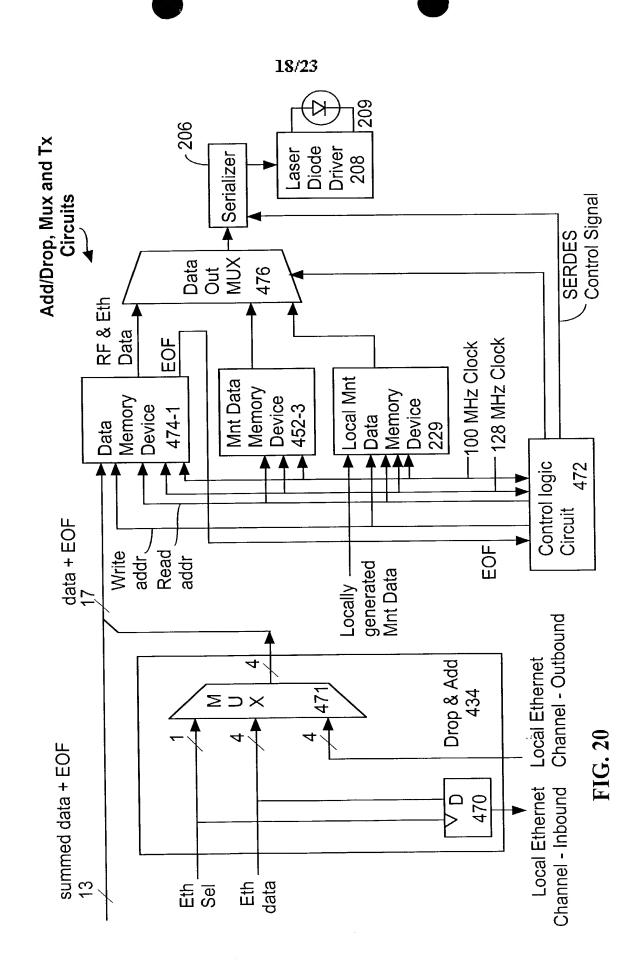


FIG. 18



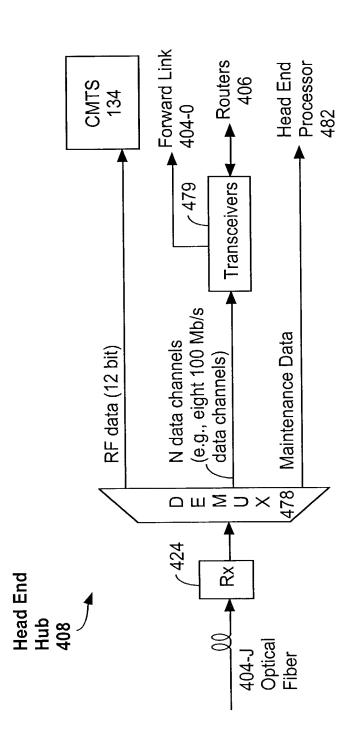


FIG. 2

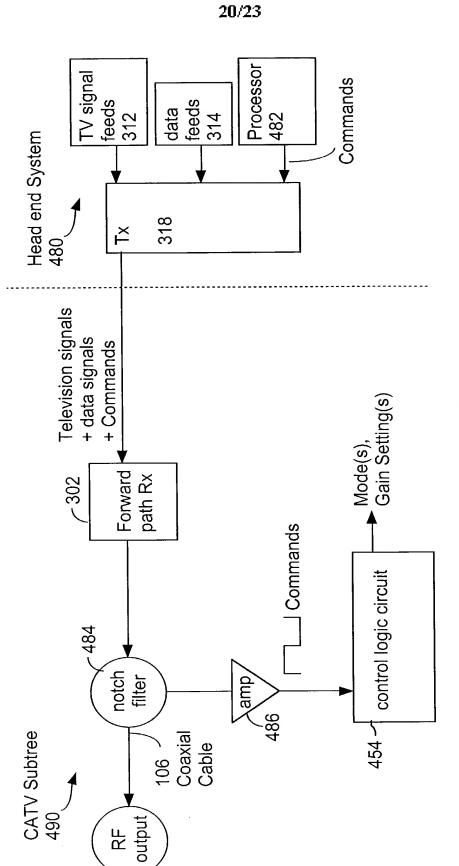
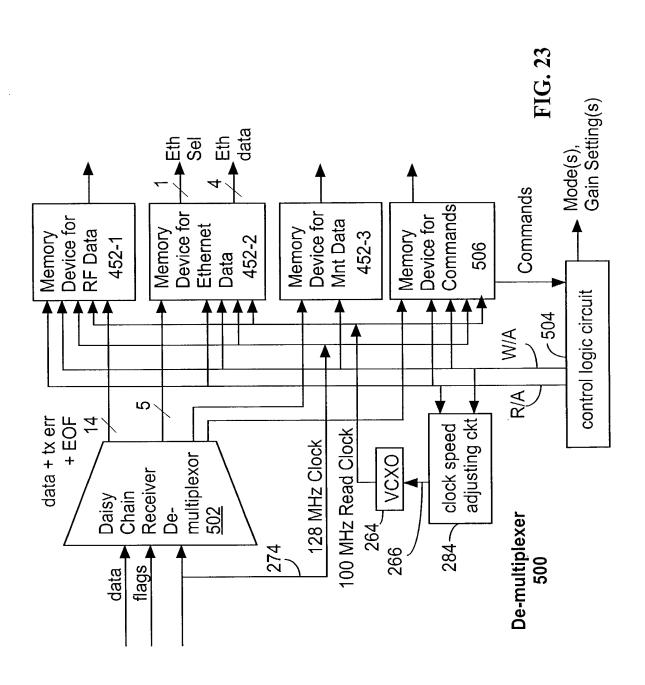
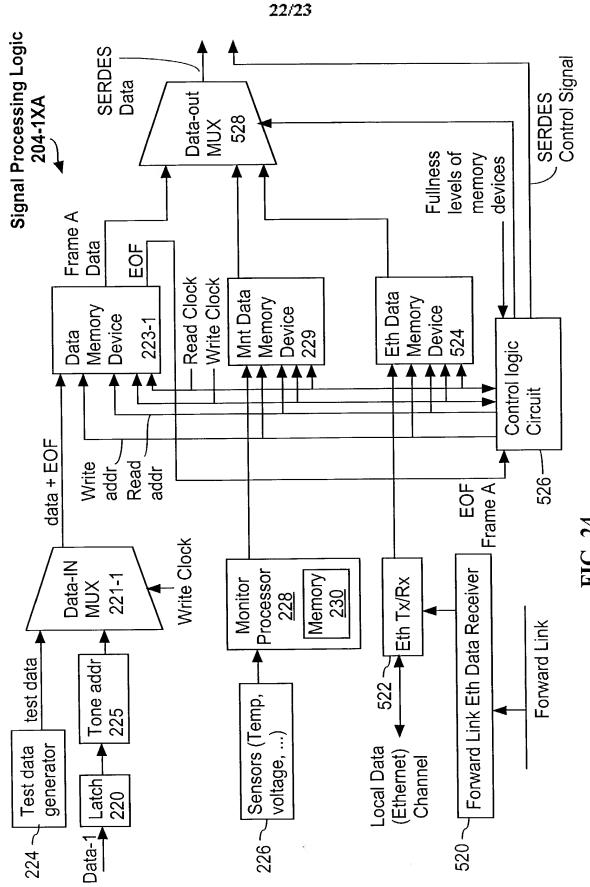


FIG. 22





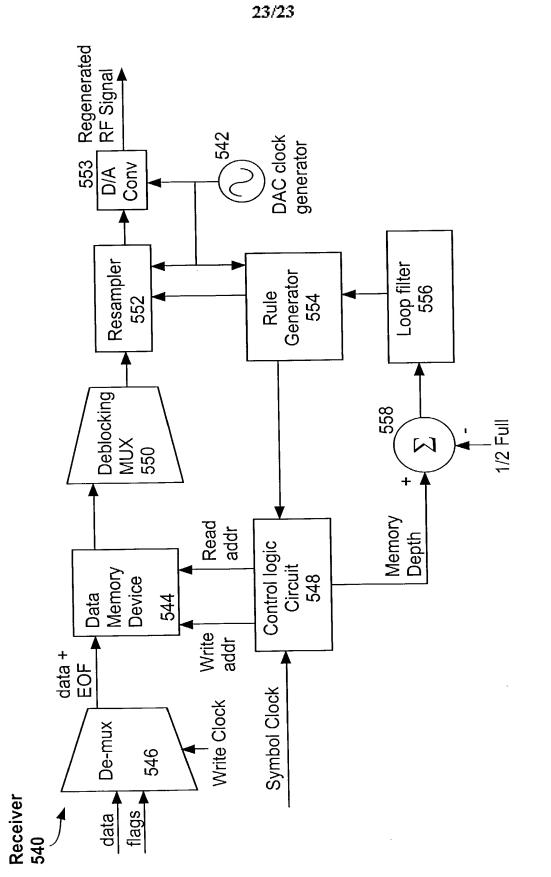


FIG. 25